REMARKS

The Examiner rejected claims 3, 4, 6, 8, 11-13, and 17 under 35 U.S.C. §112, second paragraph as being indefinite because the mathematical expressions were unclear as to what the variables/notations in the expressions are. We have amended those claims to address the Examiner's concerns.

We have also amended claim 1 to specify that the data processing system comprises a plurality of arithmetic units and the results from respective arithmetic units are combined using at least one finite field adder.

The Examiner rejected claims 1-6, 9-12, and 14-17 under 35 U.S.C. §102(b) as being anticipated by U.S. 6,061,826 to Thirumoorthy et al.

We note that Thirumoorthy et al. disclose an error computation processor comprising only one finite field multiplier 78 and one finite field adder 80, as shown in their Fig. 4a. Therefore, the processor carries computations in a serial fashion, as indicated in the description (e.g. see column 7, lines 46 to 56). As a result, the processor determines the error locator polynomial in 2t (t+3) cycles (see column 5, line 45 to 47), and determines the error evaluator polynomial in 2t (t+1) clock cycles (see column 5, lines 59 to 61). In contrast, the present claimed invention recites "a plurality of arithmetic units" and "at least one finite field adder for combining respective finite arithmetic calculation results of respective current finite field calculations of at least two arithmetic units." That is, the claimed invention uses a parallel implementation to perform its calculations and thus can perform them much faster. The described embodiment, which is an example of the claimed architecture, calculates the error locator polynomial in 3x2t (i.e. 6t) clock cycles (see paragraph 0064 of the present application as published), and it calculates the error evaluator polynomial in t clock cycles (see paragraph 0073 of the present application as published). In short, Thirymoorthy et al. do not disclose or suggest a data processing system comprising a plurality of arithmetic units as recited in claim 1.

The Examiner rejected claims 1-17 under 35 U.S.C. §102(e) as being anticipated by U.S. 7,003,715 to Thurston.

Thurston appears to describe apparatus shown in Fig. 12 for calculating the error locator polynomial. The apparatus appears to include four Galois field units (GFU's), one of which is shown in Fig. 13. Each GFU includes one GF multiplier 160 and one GF adder 164. However, Thurston does not indicate that respective results generated by GFU's are combined using at least one finite field adder, as recited in the present claims. Furthermore, Thurston's implementation is inflexible in that it is specifically optimized for decoding BCH-3 codes (see column 22, lines 30 to 31). The apparatus for calculating the error locator polynomial is not clearly extensible for decoding BCH codes of greater degree. In contrast, the apparatus of the present claimed invention, shown for example in Figs. 1 and 4, which includes finite field adders 120, 122 and 124 for combining respective results from respective arithmetic units, can be easily extended to be applicable at least to BCH codes of a greater degree.

For the reasons stated above, we believe that the claims are allowable and therefore ask the Examiner to allow them to issue.

Please apply any charges not covered, or any credits, to Deposit Account No. 08-0219.

Respectfully submitted,

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